AMENDMENTS TO THE CLAIMS

Please cancel claims 3-4, 6-7, 10-24, 26, and 32 without prejudice. Kindly amend claims 1-2, 5, 8-9, 25, 27-30, and 33, and add new claim 34 as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended) An apparatus for executing an MMX PSADBW instruction, comprising:

subtractors, for generating packed differences of packed operands of the instruction and for generating ~~carry~~ borrow bits associated with each of the packed differences;

inverters, coupled to said subtraction logic, for generating an inverse of each of said packed differences;

multiplexers, coupled to said inverters and said subtraction logic, each for selecting as an output said packed difference if said associated ~~carry~~ borrow bit indicates the packed difference is positive, and for selecting as said output said inverse if said associated ~~carry~~ borrow bit indicates the packed difference is negative; and

a first adder, coupled to said multiplexers, configured to add said outputs of said multiplexers to generate a first sum and a first carry;

a second adder, coupled to said subtractors, configured to add said borrow bits to generate a second sum and a second carry in parallel with said first adder generating said first sum and carry;

a third adder, coupled to said first and second adders, configured to add said first and second sums and carries to generate a result of the PSADBW instruction.

~~adders, coupled to said multiplexers, for adding said carry bits and said outputs of said multiplexers to generate a result of the instruction.~~

2. (currently amended) The apparatus of claim 1, further comprising:

an instruction type input, for specifying whether the PSADBW instruction or a multiply instruction is being executed by the apparatus; ~~and~~

second multiplexers, coupled to said first adder, configured to provide said outputs of said first multiplexers to said first adder if said instruction type specifies the PSADBW instruction and to provide a first set of partial products to said first adder if said instruction type specifies the multiply instruction; and

third multiplexers, coupled to said second adder, configured to provide said borrow bits to said second adder if said instruction type specifies the PSADBW instruction and to provide a second set of partial products to said second adder if said instruction type specifies the multiply instruction.

~~second multiplexers, coupled to said first multiplexers, for providing to said adders said carry bits and said first outputs of said first multiplexers if said instruction type input specifies the PSADBW instruction, and for providing partial products if said instruction type input specifies a multiply instruction.~~

3-4. (canceled)

5. (currently amended) The apparatus of ~~claim 4~~claim 2, wherein said third adder is also selectively employed to generate a sum of first and second product results generated by said first and second adders, rather than said result of the PSADBW instruction, if said instruction type specifies the multiply instruction~~of said at least one multiply instruction~~.

6-7. (canceled)

8. (currently amended) The apparatus of claim 1, wherein each of said ~~carry~~ borrow bits comprises a Boolean zero value if said associated packed difference is positive and comprises a Boolean one value if said associated packed difference is negative.

9. (currently amended) The apparatus of claim 1, further comprising:

a plurality of storage elements, for storing said ~~carry~~ borrow bits.

10-24. (canceled)

25. (currently amended) A method for executing an MMX PSADBW instruction by a microprocessor, comprising:

generating packed differences of packed operands of the instruction and generating ~~carry~~ borrow bits associated with each of the packed differences;

for each of the packed differences, determining whether the ~~carry~~ borrow bit indicates the packed difference is positive or negative;

for each of the packed differences, selecting a value in response to said determining, said value comprising the packed difference if the associated ~~carry~~ borrow bit is positive and a complement of the packed difference if the associated ~~carry~~ borrow bit is negative; ~~and~~

adding said selected values to generate a first sum and a first carry;

adding said borrow bits to generate a second sum and a second carry in parallel with said adding said selected values to generate a first sum and a first carry;

adding ~~the values selected and the carry bits~~ said first and second sums and said

first and second carries to generate a result of the instruction; and

storing said result in a register of the microprocessor.

26. (canceled)

27. (currently amended) The method of claim 25, further comprising:

determining whether the PSADBW instruction or a multiply instruction is being executed;

said adding said selected values to generate a first sum and a first carry and said adding said borrow bits to generate a second sum and a second carry in parallel with said adding said selected values to generate a first sum and a first carry, ~~adding the values selected and the carry bits~~ if the PSADBW instruction is being executed; and

adding first partial products to generate said first sum and said first carry and adding second partial products to generate said second sum and said second carry in parallel with said adding said first partial products, if the multiply instruction is being executed.

28. (currently amended) The method of claim 25, further comprising:

storing the ~~carry~~ borrow bits, after said generating the ~~carry~~ borrow bits.

29. (currently amended) The method of claim 25, further comprising:

translating the PSADBW instruction into ~~at least~~ first and second microinstructions, prior to said generating.

30. (currently amended) The method of claim 29, further comprising:

said generating, said determining, and said selecting in response to said first microinstruction; and

said adding said selected values to generate a first sum and a first carry, said adding said borrow bits to generate a second sum and a second carry, and said adding said first and second sums and said first and second carries, in response to said second microinstruction.

31. (original) The method of claim 25, wherein said selecting is performed in parallel for the packed differences.

32. (canceled)

33. (currently amended) A computer program product embodied on a computer-readable storage medium for use with a computing device~~data signal embodied in a transmission medium~~, comprising:

a computer-readable storage medium, having computer-readable program code embodied in said medium for providing an apparatus for executing an MMX PSADBW instruction, said program code comprising:

first program code for providing subtractors, for generating packed

differences of packed operands of the instruction and for generating ~~carry~~ borrow bits associated with each of the packed differences;

second program code for providing inverters, coupled to said subtraction logic, for generating an inverse of each of said packed differences;

third program code for providing multiplexers, coupled to said inverters and said subtraction logic, each for selecting as an output said packed difference if said associated ~~carry~~ borrow bit indicates the packed difference is positive, and for selecting as said output said inverse if said associated ~~carry~~ borrow bit indicates the packed difference is negative; ~~and~~

fourth program code for providing a first adder, coupled to said multiplexers, configured to add said outputs of said multiplexers to generate a first sum and a first carry;

fifth program code for providing a second adder, coupled to said subtractors, configured to add said borrow bits to generate a second sum and a second carry in parallel with said first adder generating said first sum and carry; and

sixth program code for providing a third adder, coupled to said first and second adders, configured to add said first and second sums and carries to generate a result of the PSADBW instruction.

~~adders, coupled to said multiplexers, for adding said carry bits and said outputs of said multiplexers to generate a result of the instruction.~~

34. (new) The apparatus of claim 1, wherein said third adder comprises:

a fourth adder, for adding said second sum and said second carry and said first sum to generate a third sum and third carry;

a fifth adder, for adding said third sum and said third carry and said first carry to generate a fourth sum and a fourth carry; and

a sixth adder, for adding said fourth sum and said fourth carry to generate said result.